Amendments to the Specification:

Please replace the paragraph beginning on page 9, line 16, with the following rewritten paragraph:

The data transfer control device 10 comprises physical-layer (PHY) circuitry 14, link-layer circuitry 20, SBP-2 circuitry 22, an interface circuit 30, a buffer management circuit 38, and a packet buffer 40 (data buffer). It also comprises a CPU 42 and the flash memory 44 (EEPROM). A processing module (program) ~~therefor~~ therefore is stored in the flash memory 44, comprising firmware 50 that is executed by the CPU 42 (generally speaking: a processor). Note that the data transfer control device 10 of this embodiment does not necessarily ~~comprises~~ comprise all of the circuit blocks and function blocks shown in Fig. 6; some of them can be omitted.

Please replace the paragraph beginning on page 11, line 16, with the following rewritten paragraph:

The firmware 50 is a program comprising various processing ~~module~~ modules (processing routines) that run on the CPU 42, and the protocols for layers such as the transaction layer are implemented by this firmware 50 and the CPU 42 or the like that is hardware.

Please replace the paragraph beginning on page 14, line 2, with the following rewritten paragraph:

A program write completion mark is stored in the program write completion mark area. This mark is used to indicate whether the program has been written normally to the SBP-2 firmware program area (generally speaking: information indicating whether or not the data transfer control program information has been written normally to the rewrite ~~area.~~ area).